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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

PATEL, ISHWARBHAI B

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 03/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/053,362

Applicant(s)

BECKER ET AL.

Examiner

Ishwar (I. B.) Patel

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 16-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 January 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-15, drawn to a multi chip module substrate, classified in class 174, subclass 262.
 - II. Claims 16-20, drawn to a method of repairing an electronic package, classified in class 29, subclass 846.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product does not need the steps of identifying the defect or the step of isolating the via or the step of firing the package.
3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Kevin R. Casey (32,117) on February 20, 2003, a provisional election was made without traverse to prosecute the invention of a multi chip module substrate, claims 1-15. Affirmation of this election must be made by applicant in replying to this Office action. Claims 16-20 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

6. The drawings are objected to because the figures are improperly cross hatched. All of the parts shown in section, and only those parts, must be cross hatched. The cross hatching pattern should be selected from those shown on page 600-114/115 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

"said circuit lines are within said chip site" and "said repair lines are within said chip site" is not clear. Is it between the chip sites or inside the circuit board?

As described in the specification the circuit lines and repair lines are embedded inside the circuit board.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seyama US Patent No. 4,912,603 in view of Nathan et al., US Patent No. 5,917,229, hereafter Nathan and Thornberg, US Patent No. 5,360,948.

Regarding claim 1, Seyama discloses a multi chip module substrate comprising;

a plurality of chip sites (printed wiring board mounting high density semiconductor devices, see figure 8 and 9, column 5, line 50-60), each having

a plurality of signal vias (vias in region R1, see figure 9, which may include signal, power and ground via, see figure 8 and 9, column 6, line 1-35), and

a plurality of repair vias (via in region R2, see figure 9, column 6, line 1-35);

a circuit line net having a plurality of circuit lines, each said circuit line extending between and intended to electrically connect selected signal via (there will inherently be circuit lines including the circuit lines 8 as shown in figure 9); but

fails to disclose a repair line net having a plurality of groups of repair lines, each said repair line extending between and electrically connecting a repair via of one said chip site and repair via of another said chip site.

However, such prepatterned lines for future changes, as disclosed by Janai and Thornberg, are known in the art and can be provided depending upon the specific situation for quick change or repair of the defective elements.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board assembly of Seyama with a repair line net having a plurality of groups of repair lines, each said repair line extending between and electrically connecting a repair via of one said chip site and repair via of

another said chip site as taught by Janai and Thornberg, in order to facilitate quick change or repair of the circuit board.

Regarding claim 7, though Seyama does not disclose the jumper connections, such prepatterned connections can be provided depending upon the specific requirement as applied to claim 1 above for quick repair / changes in the circuit boards.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the modified circuit board assembly of Seyama with the jumper connections, as taught by Janai and Thornberg in order to have quick change or repair into the circuit board.

Regarding claim 2 and 8, though Seyama does not disclose the circuit lines and repair line within the chip sites, such line inside the boards, multilayer boards, as shown by Janai and Thornberg is known in the art, to be able to have more components on the board.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the modified circuit board assembly of Seyama with the circuit lines and repair line within the chip sites in order to have increased component density of the board.

Regarding claims 3, 5, 9 and 11 Seyama further discloses the repair vias are outside of and surrounding an array of said signal via, see figure 9, modification pad outside the terminal pads region, column 6, line 1-20.

Regarding claim 4, 6, 10 and 12 Seyama further discloses the identical chip sites.

Regarding claims 13, 14 and 15, the applicant is claiming the number of repair vias in each chip site and number of repair lines and number of group of repair line in relation to the number of chip sites.

Though, the modified assembly of Seyama does not disclose such specific relations, those elements will be provided based on the need for that specific assembly to have enough repair vias and lines for quick change or repair of the circuit board.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the modified circuit board assembly of Seyama with the number of repair vias in each chip site and number of repair lines and number of group of repair line in relation to the number of chip sites as claimed in claims 13, 14 and 14, in order to have enough repair vias and repair lines for quick change or repair of the circuit board.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Evans et al., disclose prepatterned traces within the circuit board for customizing the circuit design.

Grobman et al., disclose engineering change ring pattern for change capability.

Nathan et al., disclose the use of fuse / antifuse for changes to reduce the programming time.

Weigler et al., disclose the programmable conductive links placed on the top layer of the substrate for customization.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (8:30 - 5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

ibp
March 9, 2003


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